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(84) Designated contracting states:	(74) Representative:

(54) CONTROL SYSTEM FOR ACCESSING MEMORY DEVICE

(57) Abstract:

PURPOSE: To accelerate accessing at high speed, by dividing a memory device connected to a common bus into N sets, and providing a circuit to set the transmission/reception timing of data on each set, and a circuit to set an instruction which suppresses the accessing.

CONSTITUTION: The memory device 2 connected to the common bus 3 is divided into N sets, and the circuit 210 which sets the transmission/reception timing of a readout data, or a write data, and the circuit 211 which sets the instruction to suppress the accessing to each of the memory devices 21W2N, are provided. Control is applied on the plural sets of the memory devices except the memory device being instructed to suppress the accessing by the circuit 211 among the memory devices 21W2N, so as to access with a set transmission/reception timing. Therefore, it is possible to perform the accessing efficiently even in a computer system being provided with a two-way common bus capable of accessing in a single accessing action and with a data width smaller compared with a data length desired to access.